ABSTRACT

Multiphase clock generators and methods are provided. A multiphase clock generator has a first clock divider for generating a first-phase clock signal from a first input clock signal. A first logic gate is connected to an output port of the first clock divider. A second clock divider is connected to an output port of the first logic gate. The second clock divider is for generating a second-phase clock signal from the first input clock signal. A second logic gate is connected to an output port of the second clock divider. A third clock divider is connected to an output port of the second logic gate. The third clock divider is for generating a third-phase clock signal from a second input clock signal.